Section 102(b) Rejection:

The Office Action rejected claims 21 and 22 under 35 U.S.C. § 102(b) as being anticipated by Taylor et al. (U.S. Patent 5,834,958) (hereinafter "Taylor"). As set forth in more detail below, Applicants respectfully traverse this rejection.

Taylor does not teach the transistor is configured to sink current from the voltage rail when the transistor is on to decrease the voltage on the voltage rail below the first voltage level. Claim 21 recites that the transistor coupled to the voltage rail and to the shunt regulator is configured to sink current from the voltage rail when the transistor is on to decrease the voltage on the voltage rail below the first voltage level, which causes the voltage divider to apply an input voltage to the shunt regulator that is less than the reference voltage of the shunt regulator, which then causes the shunt regulator to turn off, which then causes the transistor to turn off. In contrast, Taylor teaches a guard circuit configured to block the output of a supply voltage monitor until the supply voltage has reached a level at which the supply voltage monitor can reliably operate (Taylor -- col. 1, lines 61-67). According to Taylor, when the supply voltage reaches a level at which the supply voltage monitor can reliably operate, the shunt regulator U2 conducts and causes output transistor Q2 to communicates the supply voltage status indication provided by the supply voltage monitor U1 (Taylor -- col. 2, lines 1-21). When the supply voltage VCC reaches the predetermined voltage at which other electronic circuitry can safely operate, the supply voltage monitor U1 pulls the base of PNP output transistor Q2 to a low voltage, causing Q2 to turn on and drive a high voltage on the PON output to indicate to the other electronic circuitry of the system that power is now on (Taylor -- col. 2, lines 36-40; col. 4, lines 33-42).

Thus, Taylor's output transistor Q2 is clearly not configured to sink current from the voltage rail when the transistor is on to decrease the voltage on the voltage rail below the first voltage level, which causes the voltage divider to apply an input voltage to the shunt regulator that is less than the reference voltage of the shunt regulator, which then causes the shunt regulator to turn off, which then causes the transistor to turn off, as

recited in claim 21. In fact, such operation is counter to the teachings of Taylor. The purpose of Taylor's output transistor Q2 is to assert a digital PON signal to the system when the supply voltage VCC has reached a level appropriate for other circuitry to begin operation. When Q2 turns on, the PON signal is asserted by the voltage drop across R6 (Taylor -- col. 4, lines 33-42). If while the power supply was on, Taylor's output transistor then caused the supply voltage level to decrease low enough to turn off the shunt regulator and output transistor, the PON signal would go low and effectively turn off the rest of the system. Taylor's guard circuit clearly does not operate in that manner. In fact, Taylor it would be completely counter to the intended purpose of Taylor's power on circuit if the output transistor decreased the supply voltage when on such that the transistor turned off, which would turn off the PON signal. Thus, not only does Taylor fail to anticipate claim 21, Taylor teaches away from Applicants' invention as recited in claim 21.

Section 103(a) Rejections:

The Office Action rejected claims 1, 3-12 and 14-22 under 35 U.S.C. § 103(a) as being unpatentable over Taylor in view of Budelman (U.S. Patent 5,629,608). Applicants respectfully traverse this rejection in light of the following remarks.

Taylor in view of Budelman does not teach or suggest a clamping circuit comprising a clamping stage coupled to a detecting stage and configured to reduce the supply voltage in response to being activated by the detecting stage, as recited in claim 1. As discussed above in regard to the section 102(b) rejection, Taylor's guard circuit is not configured to reduce the supply voltage. In Taylor, when the supply voltage reaches a predetermined level, transistor Q2 turns on and drives the PON signal to a high voltage level. The purpose of the PON signal is to indicate that the supply voltage has reached a high enough level for other circuits to begin operation. It would be completely counter to Taylor's intended purpose to reduce the supply voltage once the PON signal has been asserted.

Furthermore, Taylor in view of Budelman does not teach or suggest that the switching regulator is configured to provide a termination voltage to the system memory, as recited in claim 1. The Examiner states that bus 310 in Budelman is a termination voltage supplied to the system memory by the switching regulator. However, Budelman teaches that bus 310 is a bus for transferring information, not providing a termination voltage to the system memory (Budelman -- col. 3, lines 62-63). Moreover, bus 310 is not provided by the switching regulator. Nor is power bus 370 of Budelman a termination voltage supplied to the system memory by the switching regulator. Power bus 370 is the power supply bus for components in Budelman's computer system. Although power bus 370 does provide power to the system memory, Budelman does not teach that it provides a termination voltage to the system memory. The voltage supplied on a computer system power bus is not necessarily the same as a termination voltage supplied to system memory.

Moreover, Taylor in view of Budelman does not teach or suggest a voltage regulator configured to provide a supply voltage to a switching regulator, as recited in claim 1. As shown in Fig. 4 of Budelman, switching regulator 420 receives its supply voltage from unregulated DC voltage 410. Thus, Budelman does not teach a switching regulator that receives a voltage supply from a voltage regulator.

In regard to claim 12, Taylor in view of Budelman does not teach or suggest clamping the voltage rail in response to detecting when the voltage rail exceeds a first voltage level so that the voltage rail does not exceed a maximum voltage level. There is no teaching in Taylor of clamping the voltage rail so that the voltage rail does not exceed a maximum voltage level.

Furthermore in regard to claim 12, Taylor in view of Budelman does not teach or suggest providing a termination voltage to system memory. The Examiner states that bus 310 in Budelman is a termination voltage supplied to the system memory by the switching regulator. However, Budelman teaches that bus 310 is a bus for transferring information, not providing a termination voltage to the system memory

(Budelman -- col. 3, lines 62-63). Moreover, bus 310 is not provided by the switching regulator. Nor is power bus 370 of Budelman a termination voltage supplied to the system memory by the switching regulator. Power bus 370 is the power supply bus for components in Budelman's computer system. Although power bus 370 does provide power to the system memory, Budelman does not teach that it provides a termination voltage to the system memory. The voltage supplied on a computer system power bus is not necessarily the same as a termination voltage supplied to system memory.

Moreover in regard to claim 12, Taylor in view of Budelman does not teach or suggest a linear regulator providing a voltage rail to a switching regulator. As shown in Fig. 4 of Budelman, switching regulator 420 receives its supply voltage from unregulated DC voltage 410. Thus, Budelman does not teach a linear regulator providing a voltage rail to a switching regulator.

The Office Action rejected claims 2 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Taylor in view of Budelman, and further in view of Lee et al. (U.S. Patent 5,920,511). Applicants assert that claims 2 and 13 are patentable for at least the reasons given above.

CONCLUSION

Applicants submit the application is in condition for allowance, and notice to that effect is requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicants hereby petition for such extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5500-64600/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☒ Marked-up Copy of Amended Claim

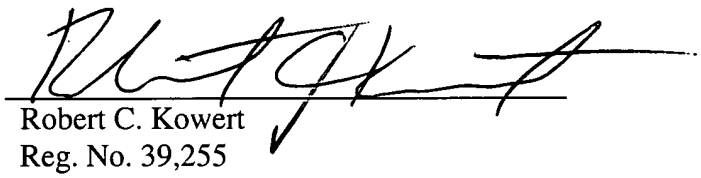
☐ Marked-up Copy of Amended Paragraph

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $

for fees ( ).

☐ Other:

Respectfully submitted,



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Date: April 29, 2003

Marked-up Copy of Amended Claim:

21. (Twice Amended) A clamping circuit configured to clamp a voltage rail in a computer system, comprising:

a voltage divider coupled to the voltage rail and to a shunt regulator, wherein the voltage divider is configured to apply an input voltage to the shunt regulator, wherein the voltage divider is configured so that the input voltage is greater than or equal to a reference voltage level of the shunt regulator when a voltage on the voltage rail is greater than or equal to a first voltage level, and wherein the voltage divider is configured so that the input voltage is less than the reference voltage level when the voltage on the voltage rail is less than the first voltage level;

the shunt regulator coupled to the voltage divider, wherein the shunt regulator is configured to turn on when the input voltage is greater than or equal to the reference voltage level and turn off when the input voltage is less than the reference voltage level; and

a transistor coupled to the voltage rail and to the shunt regulator, wherein the transistor is configured to turn on in response to the shunt regulator turning on, wherein the transistor is configured to sink current from the voltage rail when the transistor is on to decrease the voltage on the voltage rail below the first voltage level <u>while the voltage rail is being supplied by a power supply</u>, and wherein the transistor is further configured to turn off when the shunt regulator is off.